ABSTRACT

Comparison circuit for analog/digital converter

The invention pertains to a comparison circuit for an analog/digital converter. In order to reduce the effect of the offset voltages of the various comparators of the comparison circuit, voltage followers (A) and a resistor network (2) delivering at its outputs (O', $\overline{O}$'), mean voltages that are the average of those present on outputs (O, $\overline{O}$) of the comparators (C) are linked downstream of the outputs (O) of the comparators (C).

Figure 2.